IN THE CLAIMS

1. (Original) A content addressable memory (CAM) system comprising:

a ternary CAM array segmented into a plurality of array groups, each array group including a plurality of rows of ternary CAM cells; and

a plurality of first storage elements each for storing a priority of a corresponding array group.

2. (Original) The CAM system of Claim 1, wherein two or more array groups have the same priority.

3. (Original) The CAM system of Claim 1, wherein one of the rows of ternary CAM cells comprises:

a plurality of CAM cells for storing a data word; and

a plurality of mask cells for storing a local mask word.

4. (Original) The CAM system of Claim 3, wherein each data word comprises a policy statement.

5. (Original) The CAM system of Claim 4, wherein the policy statement comprises protocol information.

6. (Original) The CAM system of Claim 4, wherein the policy statement comprises type-of-service information.

7. (Original) The CAM system of Claim 4, wherein the policy statement comprises cost-of-service information.

8. (Original) The CAM system of Claim 4, wherein each local mask word includes a policy mask.

9. (Original) The CAM system of Claim 1, further comprising a plurality of second storage elements each for storing a group valid bit indicating whether an associated array group is assigned its corresponding priority number.

10. (Original) The CAM system of Claim 1, further comprising a priority table including the plurality of first storage elements.

11. (Original) The CAM system of Claim 1, further comprising an index circuit coupled to the ternary CAM array to determine the index of a location in the ternary CAM array that stores data that matches a search key.

12. (Original) The CAM system of Claim 11, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive match signals from the plurality of array groups, each match signal indicative of a result of a comparison between the search key and the data stored in the array groups, and having a plurality of outputs to provide qualified match signals for the plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified match signals, and having an output to provide the index of the highest priority location in the ternary CAM array that stores data that matches the search key in response to the qualified match signals.

13. (Original) The CAM system of Claim 12, wherein the select circuit includes means for selectively forcing non-qualified match signals to a mismatch state.

14. (Original) The CAM system of Claim 12, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the match signals from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the match signals to the priority encoder as qualified match signals in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priorities associated with array groups that have data stored that matches the search key.

15. (Original) The CAM system of Claim 14, further comprising a priority table including the plurality of first storage elements.

16. (Original) The CAM system of Claim 15, wherein the select circuit further comprises a plurality of group match flag circuits, each receiving the match signals from a corresponding array group and generating a group match flag in response thereto, wherein the group match flags are provided as select signals to corresponding rows of the priority table.

17. (Original) The CAM system of Claim 1, further comprising:

means for storing data in the array groups according to priority.

18. (Original) The CAM system of Claim 1, further comprising an address circuit coupled to the ternary CAM array to select a row of the ternary CAM cells for communicating data.

19. (Original) The CAM system of Claim 18, wherein the address circuit comprises an address decoder to select a row in one array group corresponding to the priority in response to a next free address (NFA).

20. (Original) The CAM system of Claim 19, wherein the address circuit further comprises an NFA table having a number of rows, each row for storing the NFA for a corresponding priority.

21. (Original) The CAM system of Claim 20, wherein each row in the NFA table includes an empty bit storage element for storing an empty bit indicative of whether any array group is assigned to the corresponding priority.

22. (Original) The CAM system of Claim 9, wherein each of the rows of ternary CAM cells includes a valid bit storage element for storing a valid bit indicative of whether the corresponding row of ternary CAM cells stores valid data.

23. (Original) The CAM system of Claim 9, further comprising an index circuit coupled to the valid bit storage elements to determine a next free array address for an array group and its associated priority, and further coupled to the plurality of second storage elements to determine a next free group address for the array group and its associated priority.

24. (Original) The CAM system of Claim 23, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive the valid bits from the plurality of array groups, and having a plurality of outputs to provide qualified valid bits for the

plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified valid bits, and having an output to generate the next free array address in response to the qualified valid bits.

25. (Original) The CAM system of Claim 24, wherein the select circuit includes means for selectively forcing non-qualified valid bits to a mismatch state.

26. (Original) The CAM system of Claim 24, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the valid bits from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the valid bits to the priority encoder as qualified valid bits in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the data and the priorities of the array groups.

27. (Original) The CAM system of Claim 24, wherein the index circuit further comprises:

a group priority encoder having a plurality of inputs to receive the group valid bits from each of the plurality of array groups, and having an output to provide the next free group address.

28. (Currently Amended) A method of operating a content addressable memory (CAM) system including an array of ternary CAM cells segmented into a plurality of array groups,

comprising:

storing a plurality of priorities in a plurality of storage elements each associated with one or more of the array groups, wherein each array group includes a plurality of rows of the CAM cells; and

selectively storing data in the array groups according to the priorities.

29. (Original) The method of Claim 28, wherein the selectively storing data comprises:

providing a next free address (NFA) of an available row of ternary CAM cells within an array group corresponding to one of the priorities; and

storing the data at the NFA.

30. (Currently Amended) ~~The method of Claim 29,~~ A method of operating a content addressable memory (CAM) system including an array of ternary CAM cells segmented into a plurality of array groups, comprising:

storing a plurality of priorities in a plurality of storage elements each associated with one or more of the array groups;

and

selectively storing data in the array groups according to the priorities,

wherein the selectively storing data comprises:

providing a next free address (NFA) of an available row of ternary CAM cells within an array group corresponding to one of the priorities; and

storing the data at the NFA;

and

wherein providing the NFA comprises:

generating the NFA;

storing the NFA in a corresponding row of an NFA table;

selecting a row of the NFA table using the priority; and

accessing the NFA corresponding to the priority.

31. (Original) The method of Claim 30, wherein generating the NFA comprises:

for each array group, comparing associated priorities of the data with the priority of the array group to generate an enable signal;

selectively allowing, in response to the enable signals, valid bits from corresponding array groups to participate in the generation of the NFA, the valid bits indicating whether valid data is stored in corresponding rows of each array group.

32. (Original) The method of Claim 31, wherein the selectively allowing comprises:

selectively qualifying the valid bits from each array group in response to the corresponding enable signal to generate qualified valid bits; and

generating the NFA in response to the qualified valid bits.

33. (Original) The method of Claim 31, wherein the generating the NFA further comprises:

for each array group, storing a group valid bit indicative of whether the array group is assigned to one of the priorities; and

generating a first portion of the NFA in response to the group valid bits.

34. (Original) The method of Claim 28, further

comprising:

selectively comparing a search key with data stored in the array groups.

35. (Original) The method of Claim 34, wherein the selectively comparing comprises:

comparing the search key with data stored in the array groups to generate match signals;

comparing the associated priorities of each array group that includes data that matches the search key to generate a plurality of enable signals; and

selectively qualifying the match signals in response to the enable signals to generate qualified match signals.

36. (Original) The method of Claim 35, further comprising:

generating an index of the highest priority match (HPM) in response to the qualified match signals.

Double Patenting Rejections

Claims 1 and 2 are provisionally rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over Claims 29 and 30, respectively, of co-pending and commonly owned U.S. Application No. 09/829,355, which is the parent of the present application. The Examiner states that "it would have been obvious to one of ordinary skill in the art to use a ternary CAM, as recited in the instant application, instead of a binary CAM, as recited in the copending application as a matter of design choice..."

Applicants disagree with the Examiner's general proposition that it is obvious to substitute ternary CAM cells for binary CAM cells in a CAM device. However, to expedite prosecution of the present application, Applicants submit herewith a terminal disclaimer under 37 CFR 1.321(c) to overcome the obviousness-type double patenting rejection of Claims 1 and 2 over prior Application No. 09/829,355.

Claim 1 is also provisionally rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of co-pending and commonly owned U.S. Application No. 10/000,122. The Examiner states that "it would have been obvious to one of ordinary skill in the art to use a ternary CAM, as recited in the instant application, as a CAM, as recited in the copending application because a ternary CAM has many options available to it."

Applicants disagree with the Examiner's general proposition that it is obvious to substitute ternary CAM cells for binary CAM cells in a CAM device. However, to expedite prosecution of the present application, Applicants submit herewith a terminal disclaimer under 37 CFR 1.321(c) to overcome the obviousness-type double patenting rejection of Claim 1 over prior Application No. 10/000,122.

Allowable Subject Matter

Claims 6-7, 12-16, 20-21, 23-27, and 30-33 are objected to as being dependent upon a rejected base claim, but would be allowable if re-written in independent form to include the limitations of the rejected base claim and any intervening claims.

Claims 30-33

Claim 30 has been re-written in independent form to include the limitations of base Claim 28 and intervening Claim 29, and is therefore now patentable.

Claims 31-33 depend from Claim 30 and therefore distinguish over the cited references for at least the same reasons as Claim 30.

Rejection of Claims under 35 USC §102

Claims 1-5, 8-11, 17-19, 22, 28-29, and 34-36 are rejected under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,237,061 to Srinivasan et al (Srinivasan). Applicants respectfully traverse these rejections.

Claims 1-27

Applicants' Claim 1 recites:

A content addressable memory (CAM) system comprising:

a ternary CAM array segmented into a plurality of array groups, each array group including a plurality of rows of ternary CAM cells; and

a plurality of first storage elements each for storing a priority of a corresponding array group.

Srinivasan fails to disclose or suggest the CAM system recited in Applicants' Claim 1.

Srinivasan discloses a CAM array that includes a single group of rows of CAM cells, where each row stores a CAM word and a corresponding local mask word. Referring to Srinivasan's FIG. 4, each row of Srinivasan's array 200 includes CAM cells 202 for storing a CAM word and mask cells 204 for storing a corresponding local mask word. During compare operations with a search key, each CAM word may be masked by its corresponding local mask word (see col. 4, lines 26-44). Srinivasan teaches that the local mask words may be used to indicate the prefix (e.g., priority) of one corresponding CAM word, for example, to implement CIDR addressing operations. Indeed, because each local mask word indicates the prefix or priority of only one corresponding CAM word, the CAM words must be stored in the CAM array in a predetermined order according to priority, where CAM words having the highest priority are stored in the lowest row addresses (see col. 5., lines 34-55).

First, Srinivasan fails to disclose or suggest a CAM array that is segmented into a plurality of array groups, with each array group including a plurality of rows of CAM cells, as recited in Applicants' Claim 1. Rather, as discussed above, Srinivasan discloses a CAM array having a single group of rows of CAM cells. The Examiner seems to equate a row of Srinivasan's CAM array with one of Applicants' CAM array groups. However, while the CAM array of Applicants' Claim 1 includes a plurality of array groups, each including a plurality of rows of CAM cells, Srinivasan's CAM array includes only one group of CAM cells.

Second, Srinivasan fails to disclose or suggest a plurality of storage elements each for storing a priority of a corresponding array group, as recited in Applicants' Claim 1. Thus, while each of the storage elements recited in Applicants' Claim 1 stores a priority for a plurality of rows of CAM cells

in a corresponding array group, each local mask word in Srinivasan's CAM array stores a priority for a single row of CAM cells.

The Examiner states:

> A ternary CAM array segmented into a plurality of array groups is disclosed in figure 6 as group #202. Each array group including a plurality of rows of ternary CAM cells (inherent in a ternary CAM that it has ternary CAM cells) is disclosed in figure 6 as one of the four rows in each group.
>
> A plurality of first storage elements each for storing a priority of a corresponding array group is disclosed in figure 6 as the CAM index. As discussed in column 5, lines 34-55, the groups are prioritized by length of prefix by the index.

Applicants disagree. As discussed above, Srinivasan discloses a CAM array that includes only one group of rows of CAM cells, and teaches that each local mask word stores a prefix or priority for only one corresponding row of CAM cells.

The Examiner seems to equate the four sets of binary values shown in the "CAM Entries" portion of a row in the exemplary table of Srinivasan's FIG. 6 with the array groups recited in Applicants' Claim 1. However, in contrast to the Examiner's conclusion, the four sets of binary values to which the Examiner refers are not four different entries to be stored in different rows of Srinivasan's array, but rather are binary representations of corresponding CIDR addresses shown in the "IPv4/Z" portion of the exemplary table of Srinivasan's FIG. 6. For example, referring to the first row (e.g., CAM index 7) of Srinivasan's FIG. 6, the four sets of binary values indicated by reference number 202 represent the binary equivalent of the corresponding CIDR address 209.120.0.0, and therefore the four sets of binary values (202) together form a single CAM word that is stored in the CAM cells 202 in a single row of Srinivasan's

array. Similarly, the four sets of binary values indicated by reference number 204 represent the binary equivalent of the corresponding CIDR prefix value of 13, and therefore the four sets of binary values (204) together form a single local mask word that is stored in the mask cells 204 in a single row of Srinivasan's array.

Thus, as illustrated by Srinivasan's table in FIG. 6, each local mask word represented by four sets of binary values 204 in a row may be used to indicate the prefix or priority of a single corresponding CAM word represented by four sets of binary values 202 that is stored in the same row.

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference (*Corning Glass Works v. Sumitomo Electric*, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989)). The exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102 (*Connell v. Sears, Roebuck & Co.*, 220 USPQ 193, 198 (Fed. Cir. 1983)). Thus, because Srinivasan fails to disclose or suggest a CAM system that includes "a ternary CAM array segmented into a plurality of array groups, each array group including a plurality of rows of ternary CAM cells" and "a plurality of first storage elements each for storing a priority of a corresponding array group," as recited in Applicants' Claim 1, Claim 1 is neither anticipated by nor rendered obvious in view of Srinivasan. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of Claim 1.

Claims 2-27 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Claims 28-29 and 34-36

Applicants' Claim 28 (as amended) recites:

A method of operating a content addressable memory (CAM) system including an array of ternary CAM cells segmented into a plurality of array groups, comprising:

storing a plurality of priorities in a plurality of storage elements each associated with one or more of the array groups, wherein each array group includes a plurality of rows of the CAM cells; and

selectively storing data in the array groups according to the priorities.

As discussed above with respect to Claim 1, Srinivasan fails to disclose or suggest a CAM array that is segmented into a plurality of array groups, with each array group including a plurality of rows of CAM cells. Further, as discussed above with respect to Claim 1, Srinivasan also fails to disclose or suggest a plurality of storage elements each for storing a priority of a corresponding array group, where each array group includes a plurality of rows of CAM cells to store a multitude of CAM words in the array group. Therefore, Srinivasan fails to disclose or suggest "storing a plurality of priorities in a plurality of storage elements each associated with one or more of the array groups, wherein each array group includes a plurality of rows of the CAM cells" or "selectively storing data in the array groups according to the priorities," as recited in Applicants' Claim 28. Accordingly, Claim 28 is neither anticipated by nor rendered obvious in view of Srinivasan, and therefore Applicants respectively request the Examiner to withdraw the rejection of Claim 28.

Claims 29 and 34-36 depend from Claim 28 and therefore distinguish over the cited references for at least the same reasons as Claim 28.

CONCLUSION

In light of the above amendments and remarks, it is believed that Claims 1-36 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1-36 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (415) 291-9497.

Respectfully submitted,

Dated: November 22, 2004

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CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Arlington, VA 22313 on November 22, 2004.

By: _____
William L Paradice III